Abstracts

GaAs FET characterization in a quasi-monolithic Si environment

E. Wasige, G. Kompa, F. van Raay, W. Scholz, I.W. Rangelow, R. Kassing, S. Bertram and P. Hudek. "GaAs FET characterization in a quasi-monolithic Si environment." 1999 MTT-S International Microwave Symposium Digest 99.4 (1999 Vol. IV [MWSYM]): 1889-1891 vol.4.

GaAs FET chips are planar embedded in a high resistivity silicon substrate and characterized up to 40 GHz in a coplanar environment. Hybrid interconnects (bonding wires) are replaced by thin film ones (air bridges). Small signal equivalent circuit extraction results confirm the expected low parasitic inductance values. These are reduced by more than 50% of the typical bonding wire interconnects.

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